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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/992,222	12/17/1997	WILLIAM A. HOBBS	INPA:056	3574

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EXAMINER	
JEAN, FRANTZ B	

ART UNIT	PAPER NUMBER
2155	35

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/992,222	HOBBS ET AL.	
	Examiner	Art Unit	
	Frantz B. Jean	2155	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *55-78 and 85-89* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *55-78 and 85-89* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. This office action is in response to the amendment filed on 05/20/2003. Claims 55-78 and 85-89 are pending in the application. Claims 79-84 have been canceled.

2. The drawings filed on 5/20/03 have been entered.

Claim Rejections - 35 USC 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the. invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 55-78 and 85-89 are rejected under 35 U.S.C. 103(a) as being obvious over Gates (5,701,409) in view of Carlsson et al (US# 4,053,947).

5. As for claims 55, 57-59, 62, 85, Gates teaches a system and method comprising a connector to a bus; an instruction memory to store a plurality of bus stimuli instructions (see abstract) that represent a predefined sequence of bus transactions, wherein each transaction has a plurality of transaction phases; and one or more phase generators coupled between the connector and the instruction memory, the one or more phase generators to receive the plurality of bus stimuli instructions from the instruction memory and to provide a plurality of signals on the bus

that represent the predefined sequence of bus transactions. However, Gates fails to teach storing more than one command.

Official Notice is taken with regards to the storing of multiple commands in an instruction memory for the purpose of speeding up the time needed to process instructions. It would have been obvious, to a person of ordinary skill in the art at the time the invention was made to use an instruction memory for multiple instruction, in Gates, to speed LIP processing. Gates discloses all of the claimed limitations above except the use of multiple transaction phases. Carlsson discloses a method for using multiple transaction phases in a related art to increase processing time and simplify a system. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Gates, to include multiple phase transactions, as taught by Carlsson, to increase processing time and simplify a system.

6. As per claims 56 and 87, Gates implicitly teaches a high level language.

7. As per claims 60-61, Gates implicitly teaches the instruction comprises an instruction word (col. 2, lines 40-45). Gates and Carlsson don't teach that the instruction word has a predefined length. Official Notice is taken that instruction words of predefined lengths are well known in the art. It would have been obvious to a person of ordinary skill in the art, at the time of the invention, to have used instruction words of any length into Gates' and Carlsson's because they are only a matter of computer design.

8. As for claims 63-65, they are rejected as applied above in rejecting claim 55. Gates and Carlsson don't teach what the digital logic device comprises.

Official Notice is taken that FPGA's and ASIC's are well known in the art. It would have been obvious to a person of ordinary skill in the art, at the time of the invention, to have used instruction words of any length into Gates' and Carlsson's because they are only a matter of computer design.

9. As per claims 66-70, and 72-74, Gates teaches a system comprising a connector to couple the system to a bus; an instruction memory to store a plurality of bus stimuli instructions (see abstract) that represent a predefined sequence of bus transactions, wherein each transaction has a plurality of transaction phases; and one or more phase generators coupled between the connector and the instruction memory, the one or more phase generators to receive the plurality of bus stimuli instructions from the instruction memory and to provide a plurality of signals on the bus that represent the predefined sequence of bus transactions; furthermore, Gates teaches a control portion and a data portion (col. 5 lines 27-45); therefore, Gates implicitly teaches a control logic that includes a flow logic device and also, implicitly teaches a phase engine that includes logic level translation device. In addition, it is implicitly seen that a plurality of phase engines are included in Gates since a PCI bus includes theses phases; also, Gates teaches a data memory coupled to the data portion and the data portion receives data from the bus (col. 5 lines 27-45). Moreover, it is inherently seen that the IC (phase generator) can also receive signals from the bus and phase generator that includes one digital logic device responsive to the instructions and one phase engine for controlling timing are taught by Gates (abstract; col. 2, lines 40-45). However, Gates doesn't teach that the instruction has a predefined length. Official Notice is taken that

instruction of predefined lengths are well known in the art. It would have been obvious to a person of ordinary skill in the art, at the time of the invention, to have used instruction of any length because they are only a matter of computer design. Furthermore, Gates fails to teach storing more than one command.

Official Notice is taken with regards to the storing of multiple commands in an instruction memory for the purpose of speeding up the time needed to process instructions. It would have been obvious, to a person of ordinary skill in the art at the time the invention was made to use an instruction memory for multiple instruction, in Gates, to speed LIP processing. Gates discloses all of the claimed limitations above except the use of multiple transaction phases. Carlsson discloses a method for using multiple transaction phases in a related art to increase processing time and simplify a system. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Gates, to include multiple phase transactions, as taught by Carlsson, to increase processing time and simplify a system.

10. As per claim 71, Gates implicitly teaches a high level language.

11. Regarding claims 75-78, 89, the rejection above covers all the claimed limitations disclosed in these claims. Furthermore, it must be noted that detecting a bug is implicit in Gates (see abstract).

12. As per claims 86 and 88, assembling the sequence into a binary object code and capturing an incorrect response to a legal sequence of bus transaction are implicit in Gates.

Response to Arguments

13. Applicant's arguments filed 5/20/2003 have been fully considered but they are not persuasive.

14. Applicants argued that Gates in combination with Carlsson do not teach (1) detecting a bug, (2) a predefined sequence of bus transactions, (3) a plurality of phases engines coupled between a logic device and a connector; (4), Applicants also argued that the references are not combinable.

15. Examiner respectfully submits that applicants interpretation of the prior art is inaccurate. Regarding to (1), Gates implicitly teach detecting a bug during the bus test (see abstract); regarding to (2) and (3), Gates in combination with Carlsson teach an instruction memory to store a plurality of bus stimuli instructions (see abstract) that represent a predefined sequence of bus transactions, wherein each transaction has a plurality of transaction phases; and one or more phase generators coupled between the connector and the instruction memory, the one or more phase generators to receive the plurality of bus stimuli instructions from the instruction memory and to provide a plurality of signals on the bus that represent the predefined sequence of bus transactions; furthermore, Gates teaches a control portion and a data portion (col. 5 lines 27-45); therefore, Gates implicitly teaches a control logic that includes a flow logic device and also, implicitly teaches a phase engine that includes logic level translation device. In addition, it is implicitly seen that a plurality of phase engines are included in Gates since a PCI bus includes theses phases; also, Gates teaches a data memory coupled to the data portion and the data portion

receives data from the bus (col. 5 lines 27-45). Moreover, it is inherently seen that the IC (phase generator) can also receive signals from the bus and phase generator that includes one digital logic device responsive to the instructions and one phase engine for controlling timing are taught by Gates (abstract; col. 2, lines 40-45).

According to (4), Gates and Carlsson are combinable because they belong in the same field of endeavor which is computer. Furthermore, it must be noted that the rationale to modify or combine the prior art does not have to be expressly stated in the prior art; the rationale may be expressly or impliedly contained in the prior art or it may be reasoned from knowledge generally available to one of ordinary skill in the art, cstablished scientific principles, or legal precedent established by prior case law. In re Fine, 837 F. 2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones , 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). See also In re Eli Lilly & Co ., 902 F.2d 943. 14 USPQ2d 1741 (Fed. Cir. 1990) (discussion of reliance on legal precedent); In re Nilssen , 851 F.2d 1401, 7 USPQ2d 1500, 1502 . (Fed. Cir. 1988) (references do not have to explicitly suggest combining teachings); Ex arte Clanp. 227 USPQ 972 (Bd. Pat. App. & Inter. 1985); and Ex parte Levengood , 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993) (reliance on logic and sound scientific reasoning).

Accordingly, the rejection is maintained.

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Frantz B. Jean whose telephone number is (703) 305-3970. The examiner can normally be reached on Monday thru Friday from 8:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alam R. Hosain, can be reached on (703) 308-6662. The fax phone numbers for this Group are (703) 746-7238 for After-Final, (703) 746-7239 for Official, and (703) 746-7240 for Non-Official/Draft.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**Alam.Hosain@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive

information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Frantz B. Jean
July 20, 2003
FBJ/